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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,784	02/24/2004	Gi-Young Yang	SEC.1107	2211

7590 07/01/2005

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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,784	YANG ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7* is/are allowed.

6)☒ Claim(s) *8-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by admitted prior art Fig. 1.

Regarding claim 8, admitted prior art of Fig. 1 discloses a method of determining a gate capacitance of a MOS transistor (paragraph [0009]), comprising: (a) measuring a measured capacitance and a measured dissipation factor of the MOS transistor (step 110) [see paragraph 00010], (b) setting an initial capacitance (step 130) [see paragraph [00011]], (c) calculating a calculated capacitance and a calculated dissipation factor based on the initial capacitance (step 140) [see paragraph [00011-00012]] , (d) repeating steps (b) and (c) until both the calculated capacitance is equal to the measured capacitance and the calculated dissipation factor is equal to the measured dissipation factor (step 150) [see paragraph [00012]], and (e) detecting the initial capacitance as an accurate gate capacitance of the MOS transistor when it is determined that both the calculated capacitance is equal to the measured capacitance and the calculated dissipation factor is equal to the measured dissipation factor (step 160) [see paragraph [00012]].

Regarding claim 9, admitted prior art of Fig. 1 discloses prior to step (c): measuring a direct gate current, a direct drain current, a direct gate voltage, and a direct drain voltage of the MOS transistor [see paragraph [00017] lines 1-3]; and obtaining a channel resistance and a

tunneling resistance of the MOS transistor using the direct gate current, the direct drain current, the direct gate voltage, and the direct drain voltage [see paragraph [00017] lines 3-5], wherein calculated dissipation factor is calculated in step (c) based upon the channel resistance and the tunneling resistance [see paragraph [00018].

Regarding claim 10, admitted prior art of Fig. 1 discloses the tunneling resistance is calculated by $R_1=L\ [Z_{dc}/Y_{dc}*(Z_{dc}*Y_{dc}+2)]^{1/2}$ /cosh $-1(Z_{dc}*Y_{dc}+2)$, and the channel resistance is calculated by $R_1=1/R_1\ [Z_{dc}/Y_{dc}*4*(Z_{dc}*Y_{dc}+2)]$, wherein Z_{dc} is a drain impedance obtained by dividing the direct drain voltage by the direct drain current, Ydc is a gate admittance obtained by dividing the direct gate current by the direct gate voltage, and L is a length of the MOS transistor [see paragraph [00018]].

Regarding claim 11, admitted prior art of Fig. 1 discloses the calculated capacitance is calculated by wherein D_{dc} is a direct dissipation factor, D_m is the measured dissipation factor, wherein the direct dissipation factor is calculated by wherein Cm1 is calculated by where R' is a real number; L is length of the MOS transistor, Y_{ac} denotes a gate input admittance of the MOS transistor, γ is calculated by and Z_o is calculated by, where R_s is the channel resistance, and R_t is the tunneling resistance [see paragraphs [00022 and 00019]].

Regarding claim 12, admitted prior art of Fig. 1 discloses the calculated dissipation factor is calculated by $D_{m'} = D_{dc}*(1- D_{err}(1+ D_m))$, wherein Ddc is a direct dissipation factor, Dm is the measured dissipation factor, and D_{err} is an error dissipation factor, wherein the direct dissipation factor is calculated by wherein the error dissipation factor is obtained by subtracting the measured dissipation factor from the direct dissipation factor [see paragraph [00022]].

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Long et al (6069485), Kono (6426671) and Yechuri (6560567) disclose a method and apparatus for measuring capacitance in circuit board.

Allowable Subject Matter

4. Claims 1-7 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 1, the reason for the allowance of the claim is due to specific steps on determining a gate capacitance of a MOS transistor. Since claims 2-7 depend from claim 1, they also have allowable subject matter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Patent Examiner
Art Unit 2829

JMH
June 24, 2005